CSE 2301

Spring 2021

Midterm 3 Review

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1. Fill out the next states and the diagram for the JK flipflop

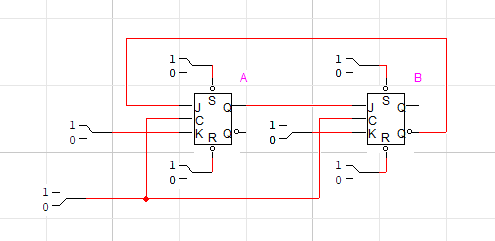
|  |  |  |  |
| --- | --- | --- | --- |
| **J** | **K** | **Q** | **Q+** |
| 0 | 0 | 0 |  |
| 0 | 0 | 1 |  |
| 0 | 1 | 0 |  |
| 0 | 1 | 1 |  |
| 1 | 0 | 0 |  |
| 1 | 0 | 1 |  |
| 1 | 1 | 0 |  |
| 1 | 1 | 1 |  |

1. Given the following K-map of the a three JK Flip Flop and input x for J1. What is the logical expression for J1? (Hint: Draw it out on scrap paper)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Q0/X |  | **00** | **01** | **11** | **10** |
| Q2/Q1 | **00** | 0 | 1 | X | X |
|  | **01** | 1 | 1 | X | X |
|  | **11** | 1 | 0 | X | X |
|  | **10** | 0 | 0 | X | X |

**J1 = \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

1. Fill out the truth table for the following circuit



|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Current | |  |  |  |  | Next | |
| QB | QA | JB | KB | JA | KA | QB | QA |
| 0 | 0 |  |  |  |  |  |  |
| 0 | 1 |  |  |  |  |  |  |
| 1 | 0 |  |  |  |  |  |  |
| 1 | 1 |  |  |  |  |  |  |

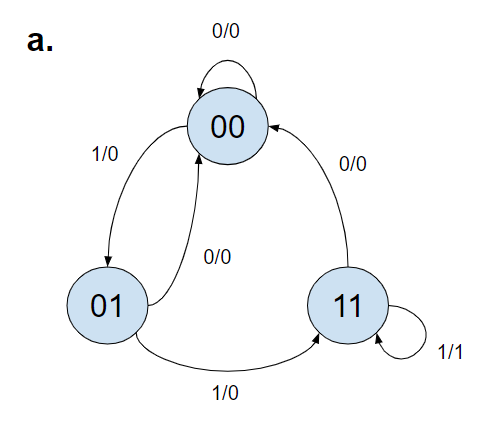
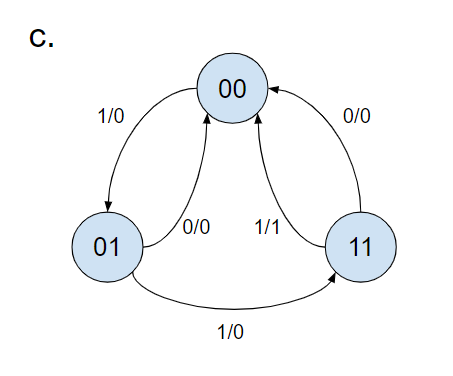
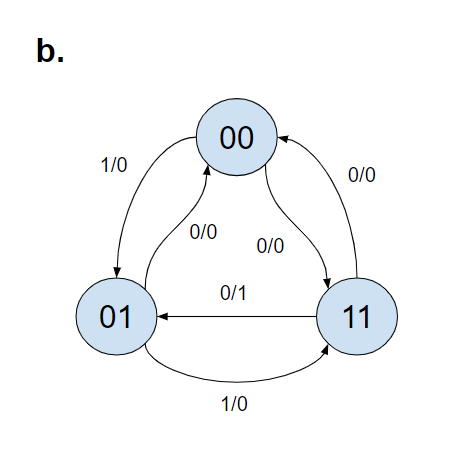
1. Draw the circuit symbols for a D flip flop and a JK flip flop.
2. We want to make a sequence detector that detects the binary sequence “111” in any given binary sequence with overlaps. There would be 3 states:

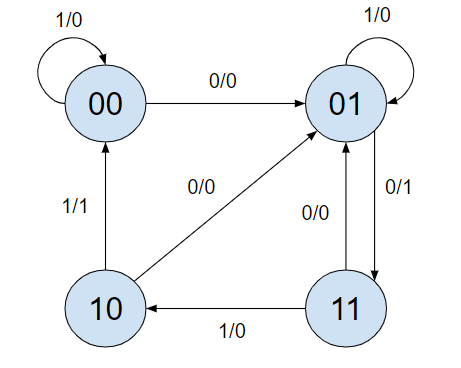
No sequence - 00

1 detected - 01

11 detected - 11

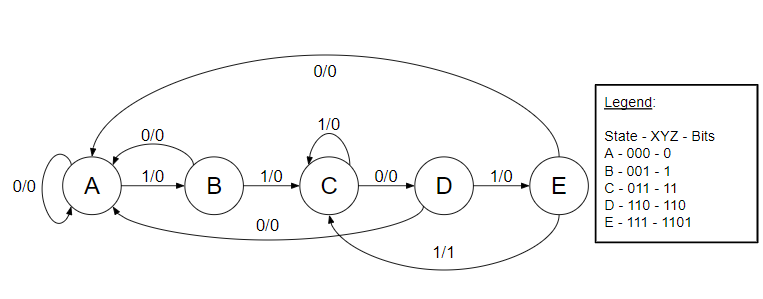
Which is the correct state diagram?

1. Given the following state diagram, fill out the state table.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Current |  | Input | Next |  | Output |
| **QA** | **QB** | **X** | **QA+** | **QB+** | **Y** |
| 0 | 0 | 0 |  |  |  |
| 0 | 0 | 1 |  |  |  |
| 0 | 1 | 0 |  |  |  |
| 0 | 1 | 1 |  |  |  |
| 1 | 0 | 0 |  |  |  |
| 1 | 0 | 1 |  |  |  |
| 1 | 1 | 0 |  |  |  |
| 1 | 1 | 1 |  |  |  |

1. The state diagram below is for detecting the sequence “11011” where overlaps can occur. This question is much harder than you will likely see on the exam.



Fill in the chart below to implement this sequence detector on JK flip-flops.

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **X** | **Y** | **Z** | **Input** | **X+** | **Y+** | **Z+** | **JX** | **KX** | **JY** | **KY** | **JZ** | **KZ** |
| 0 | 0 | 0 | 0 |  |  |  |  |  |  |  |  |  |
| 0 | 0 | 0 | 1 |  |  |  |  |  |  |  |  |  |
| 0 | 0 | 1 | 0 |  |  |  |  |  |  |  |  |  |
| 0 | 0 | 1 | 1 |  |  |  |  |  |  |  |  |  |
| 0 | 1 | 0 | 0 |  |  |  |  |  |  |  |  |  |
| 0 | 1 | 0 | 1 |  |  |  |  |  |  |  |  |  |
| 0 | 1 | 1 | 0 |  |  |  |  |  |  |  |  |  |
| 0 | 1 | 1 | 1 |  |  |  |  |  |  |  |  |  |
| 1 | 0 | 0 | 0 |  |  |  |  |  |  |  |  |  |
| 1 | 0 | 0 | 1 |  |  |  |  |  |  |  |  |  |
| 1 | 0 | 1 | 0 |  |  |  |  |  |  |  |  |  |
| 1 | 0 | 1 | 1 |  |  |  |  |  |  |  |  |  |
| 1 | 1 | 0 | 0 |  |  |  |  |  |  |  |  |  |
| 1 | 1 | 0 | 1 |  |  |  |  |  |  |  |  |  |
| 1 | 1 | 1 | 0 |  |  |  |  |  |  |  |  |  |
| 1 | 1 | 1 | 1 |  |  |  |  |  |  |  |  |  |

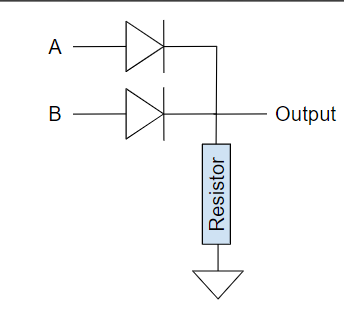
1. True or False? 5400 Series chips have a wider operating range of temperatures and voltages than the 7400 Series chips?

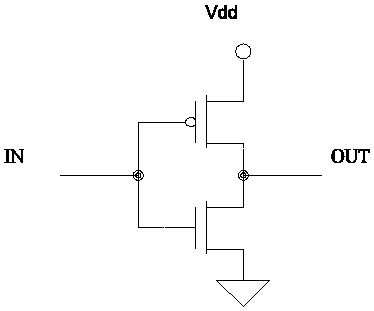
True False

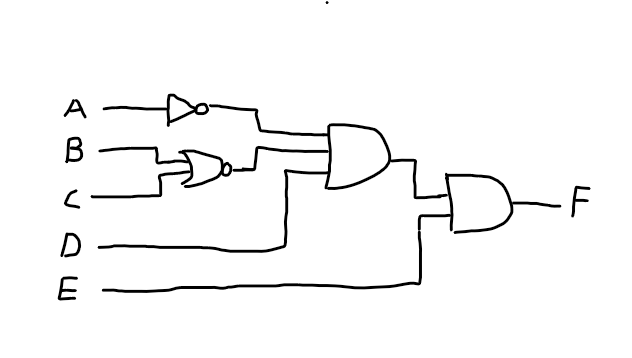
1. True or False? Shifting the contents of a loaded register to the left divides by two.

True False

1. Given the bit sequence “11001011011010,” how many times (including overlaps) does the subsequence “1011” occur?
2. 4
3. 2
4. 3
5. 0
6. What is the temperature range of the 7400 Series?
7. -40°C to 85°C
8. -55°C to 125°C
9. 0°C to 100°C
10. -273.15 °C to 1200°C
11. What does PRBS stand for?
12. Practically Random Binary Sequence
13. Proto Realistic Board Solder
14. Pseudo Remote Banana Stand
15. Pseudo Random Binary Sequence
16. How many flips flops do you need to have a sequential circuit with 17 different states?
17. 3
18. 4
19. 5
20. 17
21. Which of the following is a Shift Left Logical is performed on binary number 00101?
22. 01010
23. 01011
24. 00010
25. 10010
26. What is the Diode Logic of the following circuit?



1. XOR
2. NOR
3. NAND
4. OR
5.  What is the CMOS logic of the following circuit?
6. XOR
7. NOT
8. AND
9. OR
10. There is no logic. Nothing makes sense anymore.
11. The following circuit (that I drew in MS Paint because I gave up with google images) is broken. I think there is a stuck at fault at D. In order to the input for D, what should the other inputs be set to in order to see a change at output F? If you can’t tell what the gates are, they are NOT, NOR, 3-AND, 2-AND.



1. .
2. .
3. .

E.  .